AN INVESTIGATION OF CERIA-BASED SLURRIES EXHIBITING REVERSE-PRESTONIAN BEHAVIOUR

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ABSTRACT

New slurry formulations have been developed for polishing oxide in both shallow trench isolation (STI) and inner layer dielectric (ILD) CMP processes. These formulations use cerium oxide as the abrasive, since the industry requires a higher performance from these slurries for both of these applications at sub-90nm technology nodes, compared to the traditionally used silica-based slurries.

The performance aspects of these slurries, such as the high selectivity systems for STI and the auto-stopping systems for ILD, have been described previously at several conferences. However, in this paper, a novel feature of these slurries is described. This feature is the reverse-Prestonian behaviour which shows that, as downforce pressure increases during polishing, the oxide removal rate on blanket wafers decreases. At the same time, the removal rate on pattern wafers increases, which leads to very efficient polishing. We have identified the slurry components responsible for this behaviour and by omitting these agents from the slurry, normal Prestonian behaviour can be re-established (i.e. removal rate on blanket wafers increases in proportion to an increase in pressure times velocity).

Polishing experiments are described showing which factors affect the reverse-Prestonian behaviour and possible mechanisms are discussed.

1. INTRODUCTION: STI CMP AND ILD CMP

This paper describes the development and behaviour of ceria-based CMP slurries used in two different process steps in the production of sub-90nm technology node integrated circuits. The slurries are used in the Shallow Trench Isolation (STI) CMP and Inner Layer Dielectric (ILD) CMP processes.

The STI process was developed to effectively isolate the active areas that form the transistor gates at the device level and it allows superior scalability and fulfils the planarity requirements for lithography [1], compared to earlier techniques.

One of the greatest challenges for the integration of STI structures in circuits is

to develop a well-controlled planarization process using Chemical Mechanical Polishing (CMP). CMP is carried out following the formation of the isolation structures (trenches) by etching and the filling of the trenches with a dielectric material (usually HDP CVD oxide). After the oxide deposition, there is usually substantial topography across the structure, the result being that the oxide over the active areas is thicker than that over the field areas (trench). CMP is used to reduce the topography down to the silicon nitride CMP-stop layer deposited on the active areas. An important aspect of the process is that it needs to produce minimal dishing in the trench oxide after an overpolish step to remove the oxide from the active area nitride. The selection of the polishing slurry is therefore critical.

Apart from producing low dishing, other requirements of the slurry are that it must give; fast planarization (step height removal), high selectivity (oxide to nitride) and low defectivity. Traditionally silica-based slurries have been used, but due to the increasingly stringent requirements of the evolving technology, these can no longer provide the required performance. Silica slurries show a much greater pattern dependency than the newer ceria-based slurries. Ceria slurries are becoming dominant for sub-90nm node STI polishing. Other than decreased pattern dependency, ceria slurries show greater oxide to nitride selectivity, which limits the amount of nitride erosion.

The slurries described in this paper are one-component, high selectivity ceria slurries for sub-90nm technology node device polishing [2]. These are used in one- or two-platen processes giving firstly fast planarization (step height reduction) of topography and secondly low nitride loss, minimal within-die (WID) and within-wafer (WIW) oxide and nitride layers, low oxide dishing and low defectivity.

The ILD CMP process is carried out to planarize dielectric layers, to enable multi-layer circuits to be built up with no issues for lithography at each level, due to excessive topography across the die. Standard Inner Layer Dielectric (ILD) polishing utilises an endpoint detection or a fixed time process to determine when to stop polishing. This can create non-uniformities across the oxide surface caused by both within die topography variations and within wafer polishing rate variations [3]. Incorporation of a stopping layer would help, but the standard ILD process does not use any. One way to minimise non-uniformity and also to widen the process window is to formulate an ILD slurry with auto-stopping characteristics.

An auto-stopping slurry is one that shows a moderate to high (>3000 A/min) step height removal rate (SHRR) when polishing topography, but reverts to a low (<300 A/min) removal rate of the oxide after removal of the topography (i.e. the wafer polishes like a blanket wafer). This type of slurry, when used in an optimised process, would result in effective removal of topography to leave a very planar surface. Additionally, the slurry should show very low pattern density dependency across a wide range of feature sizes and densities (up to 1000μm and an active area density range of 10-90%). The slurries described in this paper have been formulated with auto-stopping characteristics, efficient topography removal and low pattern density dependency [4, 5].

2.REVERSE-PRESTONIAN BEHAVIOUR

An interesting aspect of some of the slurries developed for STI and ILD CMP is reverse-Prestonian behaviour. The usual relationship between removal rate, pressure on the wafer and wafer rotation speed is given by Preston's equation;

$$\text{Removal rate} = Kp \times P \times V$$

Where Kp is the Preston coefficient, P is the pressure on the wafer surface and V is the relative velocity of the surface to the pad [3].

The ceria-based slurries described in this paper show a decrease in removal rate with increasing pressure and velocity (P x V), although the pressure has the most dramatic effect. The reverse-Prestonian behaviour is actually a very attractive feature, as it enables high removal rates to be obtained at lower downforce pressures, which is the direction the industry appears to be going in. Traditional silica-slurry based processes have tended to operate at higher pressures, but it seems that polishing tools with capability greater than 5psi will no longer be made available in the future (6). The use of slurries with reverse-Prestonian characteristics would benefit here. As the blanket oxide removal rate decreases with increasing pressure, the step height removal rate of topography increases, leading to very efficient polishing.

3. EXPERIMENTAL

All of the slurries described in this paper were manufactured at the Penn Yan facility of Ferro Electronic Material Systems. Oxide and nitride thicknesses were measured using a ThermaWave 3290DUV Optiprobe. Defect inspection was carried out using an Applied Materials WF-736 Orbot tool. Post-CMP cleaning was carried out using an Ontrak double-sided brush scrubber with megasonics.

2.1. Slurries for STI CMP

Polishing was carried out using a 2-platen process on an Applied Materials Mirra CMP 200mm platform. Blanket TEOS (tetraethoxy orthosilicate) and silicon nitride wafers were used to measure removal rates and SKW3 MIT854 wafers from SKW were used to generate performance and defectivity data.

Polishing endpoint was determined by time, which had been established in previous experiments. The endpoint for the first step polish was determined to be when approximately 1000 Angstroms of active oxide remained over the 4x4 mm feature and the endpoint for the second step was determined to be when the 4x4mm area active oxide had completely cleared.

2.2. ILD Slurry Development

Polishing at the Ferro Penn Yan facility was carried out using a Strasbaugh 6EC single platen 200mm platform. Polishing at the customer site was carried out on a Novellus Momentum 200mm platform. Blanket thermal oxide (Tox) wafers were used to measure removal rates and SKW 7-2 ILD wafers from SKW were used to generate performance and defectivity data in Penn Yan. The polishing endpoint was determined to be when the Up oxide had been polished down to 10,000 Angstroms thickness (on an SKW 7-2 wafer with an initial Up oxide thickness of approximately 20,000 Angstroms). At this point, the topography across the die was less than 500 Angstroms. The customers own wafers, with over 40,000A of Up oxide thickness (20,000A step height) were used at the customer site.

3. RESULTS AND DISCUSSION: STI CMP SLURRIES

Ferro have focussed on developing 1-component slurries for STI, which are highly selective to nitride. Depending on the formulation, the selectivity can vary from 15:1 to over 250:1. A 2-step process is usually employed, with a high downforce pressure topography removal step to quickly planarise the oxide surface (end-point is when around 1000 A of active oxide is left on the 4x4mm structure) and a low downforce pressure second step to finish the polish, to produce a highly uniform surface (low nitride removal and low dishing), once the polishing has stopped on nitride. The endpoint is when all of the oxide has been cleared from the 4x4mm structure. A typical process (in this case for Tizox 8297 slurry) is;

Step 1 – 7psi downforce pressure/135 rpm platen/70 seconds/150ml-min flow rate
Step 2 – 3psi downforce pressure/135rpm platen/105 seconds/150ml-min flow rate

As the topography is removed, the wafer begins to act as a blanket wafer and the removal rate decreases. The advantage of a reverse-Prestonian slurry is that a low downforce can be used to increase the removal rate in the second step, with minimal defectivity, compared to a high downforce process.

Figure 1 shows a typical reverse-Prestonian slurry, Tizox 8297, where the blanket thermal oxide removal rate decreases with increasing downforce pressure. Figure 2 shows blanket removals on HDP oxide wafers using Tizox 8297 at different downforce pressures. It is thought that the removal rate is Prestonian up to 3psi, but at downforce pressures above 3psi, the trend is reverse-Prestonian (this can be seen in figure 4 in section 4). The removal rates shown in figure 2 remain stable as the polishing time is increased, showing only a small decrease in polishing rate.

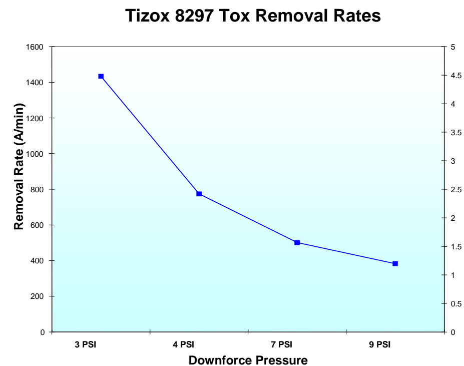

Figure 1: Reverse-Prestonian behaviour observed with Tizox 8297

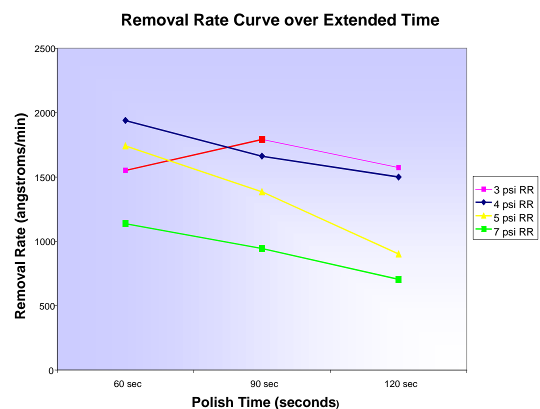

Figure 2: Effect of varying Tizox 8297 polishing time at different pressures

4. RESULTS AND DISCUSSION: ILD CMP SLURRIES

Ferro has developed a variety of slurries for ILD polishing, which exhibit either, or both, fast SHRR and auto-stopping features. The presence of auto-stopping characteristics is beneficial in widening the process window. Standard ILD polishing utilizes an endpoint detection or a fixed time process to determine when to stop

polishing. This can create non-uniformities across the oxide surface caused by both within die topography variations and within wafer polishing rate variations. Incorporation of a stopping layer would help, but the standard ILD process does not use any. One way to minimize non-uniformity and also to widen the process window is to formulate an ILD slurry with self-stopping characteristics. It can be seen that many of these ILD slurries also show reverse-Prestonian characteristics.

The examples shown in this paper are using SRS-1023, a typical auto-stopping ILD slurry that exhibits reverse-Prestonian behaviour.

It is thought that the behaviour of one of the slurry additives at different pressures is responsible for turning on, or off, the reverse-Prestonian feature. In fact, modification of the additive can easily turn Prestonian behaviour into reverse-Prestonian behaviour. This additive, or one of its by-products formed during polishing, forms a film on the oxide surface which leads to pressure-induced protection of the oxide, with the film formed being more protective at higher downforce pressures. At lower pressures (below 3psi), the protective qualities of the film decreases and the abrasive action of the ceria particles exert more influence. Below 3psi, the film exhibits no protective qualities, but the pressure is too low for the removal rate to be higher than that at 3psi, taking into account the effect of the ceria abrasive alone. Figure 3 shows a theoretical plot of removal rate vs pressure for a generic reverse-Prestonian slurry. The dashed line shows expected Prestonian behaviour in the absence of the protective film. Around 3psi, a threshold pressure exists, above which the additive film formed on the oxide becomes more efficient at protecting the surface. As pressure is further increased, the protection becomes even more effective.

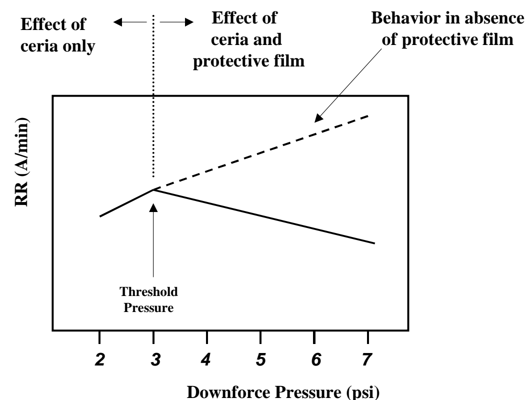

Figure 3: Reverse-Prestonian mechanism

Figure 4 shows the same trend from an evaluation of SRS-1023 at a customer site. Again, the maximum removal rate is seen around 3psi. Figure 5 shows another interesting phenomenon. It can be seen from stepwise polishing experiments on the same TEOS wafer at 3, 5 and 7psi, that at early polishing times, the behaviour is Prestonian, with 7psi giving the highest oxide removal. Only after around 20 seconds does the 3psi process lead to the highest relative oxide removal rates.

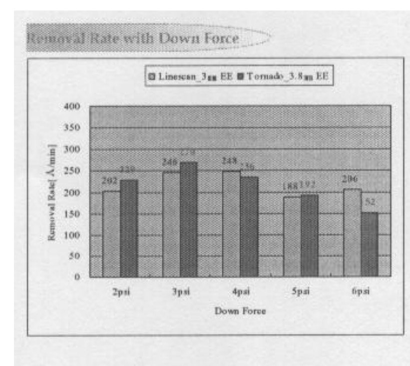

Figure 4: Oxide removal rate vs Pressure for SRS-1023

5. CONCLUSIONS

Ferro have developed slurries for polishing oxide in both STI and ILD applications, which exhibit reverse-Prestonian behaviour. The slurry component responsible for this effect has been identified and it is thought that this additive forms a film on the oxide surface, protecting it against removal and exhibiting higher efficiency at downforce pressures greater than 3psi. The main advantage of such a system is that low downforce pressures can be used, resulting in both fast oxide removal and lower defectivity, compared to traditional high downforce pressure processes.

6. REFERENCES

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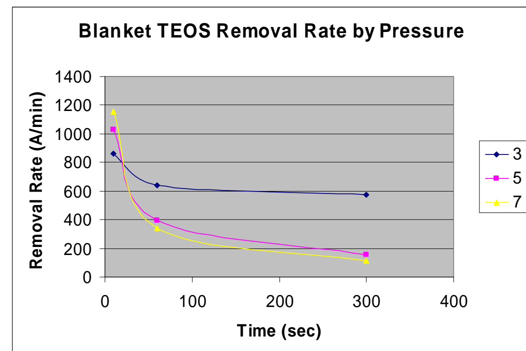

Figure 5: SRS-1023 – early polishing is Prestonian