Ceria Based Slurries for STI and “Self-Stopping” ILD Polishing: Novel Formulations and Mechanistic Understanding

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1. Introduction

STI:

In the manufacture of an integrated circuit it is critical to effectively isolate the active areas that form the transistor gates at the device level. The Shallow Trench Isolation (STI) process was developed as a more effective way of achieving this than earlier techniques, as it allows superior scalability and fulfills the planarity requirements for lithography (**1**). One disadvantage however, is the increase in process complexity.

One of the greatest challenges for the integration of STI structures in circuits is to develop a well-controlled planarization process using Chemical Mechanical Polishing (CMP). CMP is carried out following the formation of the isolation structures (trenches) by etching and the filling of the trenches with a dielectric material (usually HDP CVD oxide). After the oxide deposition there is usually substantial topography across the structure, the result being that the oxide over the active areas is thicker than that over the field areas (trench). CMP is used to reduce the topography down to the silicon nitride CMP-stop layer deposited on the active areas. An important aspect of the process is that it needs to produce minimal dishing in the trench oxide after an overpolish step to remove the oxide from the active area nitride. The selection of the polishing slurry is therefore critical.

Apart from producing low dishing, other requirements of the slurry are that it must give; fast planarization (step height removal), high selectivity (oxide to nitride) and low defectivity. Traditionally silica-based slurries have been used, but due to the increasingly stringent requirements of the evolving technology, these can no longer provide the required performance. Silica slurries show a much greater pattern dependency than the newer ceria-based slurries. Ceria slurries are becoming dominant for sub-90nm node STI polishing. Other than decreased pattern dependency, ceria slurries show greater oxide to nitride selectivity, which limits the amount of nitride erosion.

The work here describes the development of one-component, high selectivity ceria slurries for sub-90nm technology node device polishing (**2**). These are used in one- or two-platen processes giving firstly fast planarization (step height reduction) of topography and secondly low nitride loss, minimal within-die (WID) and within-wafer (WIW) oxide and nitride layers, low oxide dishing and low defectivity.

ILD:

Standard Inner Layer Dielectric (ILD) polishing utilizes an endpoint detection or a fixed time process to determine when to stop polishing. This can create non-uniformities across the oxide surface caused by both within die topography variations and within wafer polishing rate variations. One way to minimize within die and within wafer non-uniformity and also to widen the process window is to formulate ILD slurries with self-stopping characteristics.

A self-stopping ILD slurry (SSS) is one that shows a moderate to high (>3000 A/min) step height removal rate (SHRR) when polishing topography, but reverts to a low (<500 A/min) removal rate of the oxide after removal of the topography (i.e. the wafer polishes like a blanket wafer). This type of slurry, when used in an optimized process, would result in effective removal of topography to leave a very planar surface. Additionally, the slurry should show very low pattern density dependency across a wide range of feature sizes and densities (up to 1000μm and an active area density range of 10-90%).

The work here describes the development of ILD slurries that have been formulated with self-stopping characteristics, efficient topography removal and low pattern density dependency.

2. Experimental

All single-component ceria based STI and ILD slurries used in this study were manufactured and characterized at the Penn Yan facility of Ferro Electronic Material Systems. Polishing at the Ferro Penn Yan facility was carried out using an Applied Materials Mirra 200mm platform.

Oxide and nitride thicknesses were measured using a ThermaWave 3290DUV Optiprobe. Defect inspection was carried out using an Applied Materials WF-736 Orbot tool. Post-CMP cleaning was carried out using an Ontrak double-sided brush scrubber with megasonics.

3. Results and Discussion

3.1 Single Component STI Slurry

The SRS-970 slurry was formulated to have a high selectivity to nitride and give excellent WID and WIW oxide and nitride profiles. The slurry was designed with two different additives, additive A to suppress nitride removal and additive B to protect the trench oxide layer (see the mechanism in Figure 1). The slurry is designed to have a large overpolishing window and give an optimum WIW and WID profile. Using this formulation under optimum polishing conditions, the single component slurry can generate excellent results on patterned wafers (Figure 2+3).

3.2 Self-Stopping ILD Slurry

The SRS-1023 slurry was formulated to give moderate SHRR (4500 A/min) and a low thermal oxide blanket rate (<500A/min). As can be seen in figures 4, the SRS-1023 slurry shows self-stopping behavior on blanket oxide wafers, where initial polish rates are higher relative to rates at longer polish times. Patterned data is presented in figure 5, again showing the self-stopping behavior of this slurry with the planarization of the wafer. This property allows for extremely flat wafer profiles with a large overpolish window, and the ease of integration into a CMP process.

4. Slurry Manufacture and Defectivity

The capability to control the manufacture of the abrasive particle in-house is critical to the production of a consistent product. Ferro have the capability to completely control both the abrasive manufacturing process and the final product formulation. In this way, large defect-generating particles can be eliminated, whilst still retaining the particle size distribution required for optimum oxide polishing.

Typically, both total defects (including particles) and CMP-induced defects are fewer than those from a commercial silica slurry (up to three times less). CMP-induced defects include scratches, micro-scratches and pullouts.

5. Conclusions

Novel ceria-based slurries for STI and ILD CMP have been developed that meet the extremely rigorous objectives necessary for the production of sub-90nm devices. The slurries are single component products with long shelf- and pot-lives. Control of both the ceria particle manufacture and the slurry formulation in-house is critical for the production of consistent product, to minimize lot-to-lot variability and ease the way to rapid integration.

5. References

1. S.Wolf, ‘Silicon Processing for the VLSI Era volume 4 – Deep Sub-micron Processing Technology, Lattice Press, CA, pp433-474, 2002.
2. Brian Santora, Proceedings of the CMP Users Group, September, 2003.

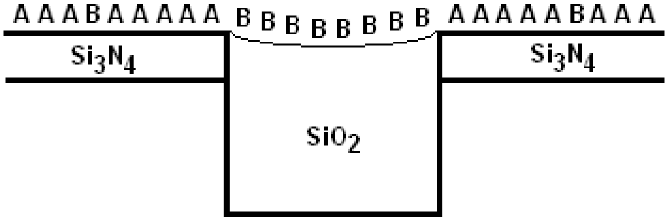

Figure 1. Proposed polishing mechanism of highly selective STI slurry. Additive A protects the silicon nitride layer, additive B protects the trench oxide.

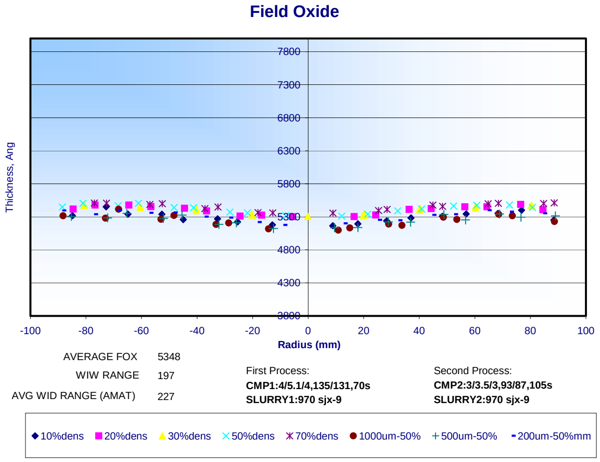

Figure 2. Single Slurry system on oxide.

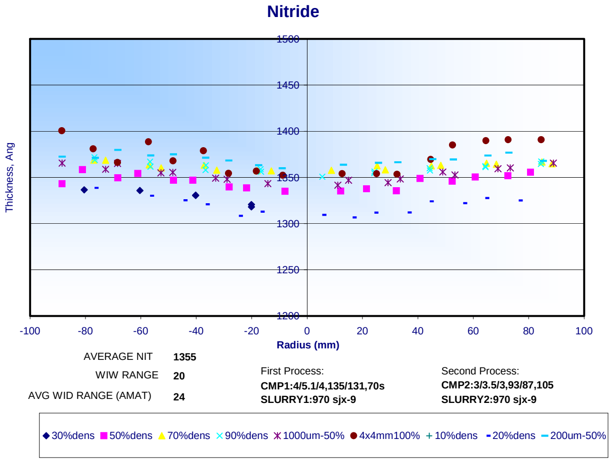

Figure 3. Single Slurry system on nitride.

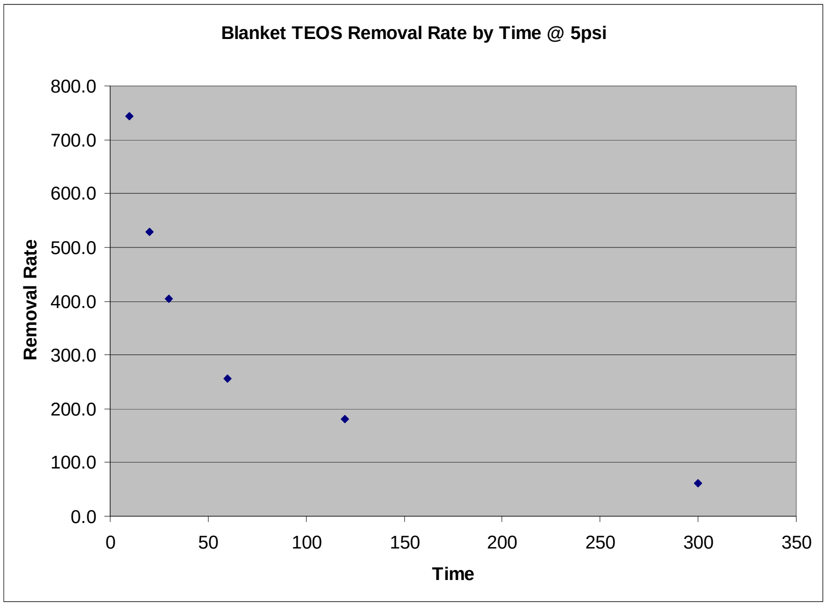

Figure 4. Blanket TEOS Removal Rate vs. polish time for SRS-1023 slurry, showing self-stopping behavior.

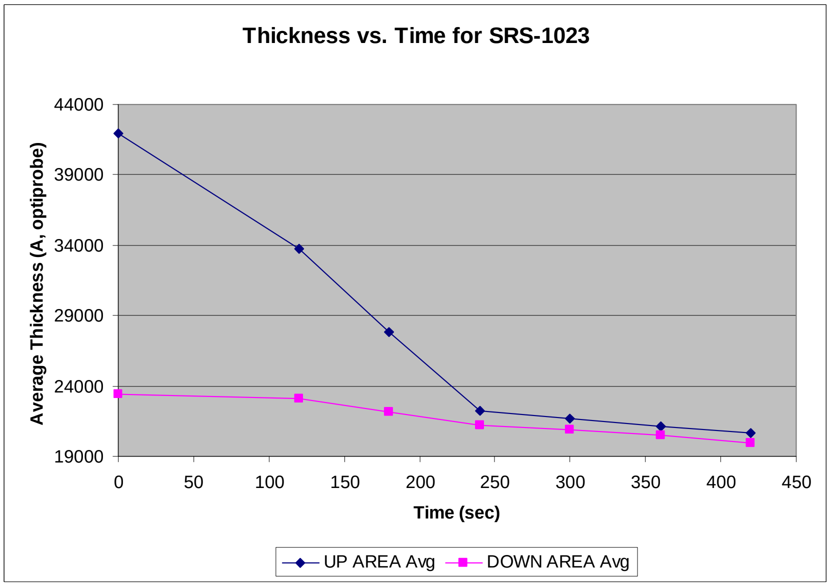

Figure 5. Patterned wafer data for SRS-1023, showing self-stopping behavior on Up and Down oxide areas.